XRT86L38EVAL

EVALUATION SYSTEM USER MANUAL

EVALUATION KIT PART LIST

This kit contains the following:

- XRT86L38EVAL Application Board
- XRT86L38 GUI Evaluation Software
- XRT86L38 420-ball TBGA
- XRT86L38EVAL User Manual
- XRT86L38 Datasheet

FEATURES

- FPGA Design Which Controls the Framer/LIU and Supports Communication Between the PCI Bridge and the XRT86L38
- PCI Bridge Connector for Easy Connection Through a Standard PC
- CD ROM Containing the GUI Software (Executable File)
- Line Interface Modules Coupled to the Receiver Inputs and Transmitter Outputs
- Power Supply Design Which uses the Supply Voltage From the PCI Bridge
- Accessible I/O Interface for Common Laboratory Equipment

SYSTEM CONFIGURATION-LAB SETUP

The XRT86L38EVAL application board is setup as a common test circuit. Figure 1 shows a simplified block diagram of the default test configuration.

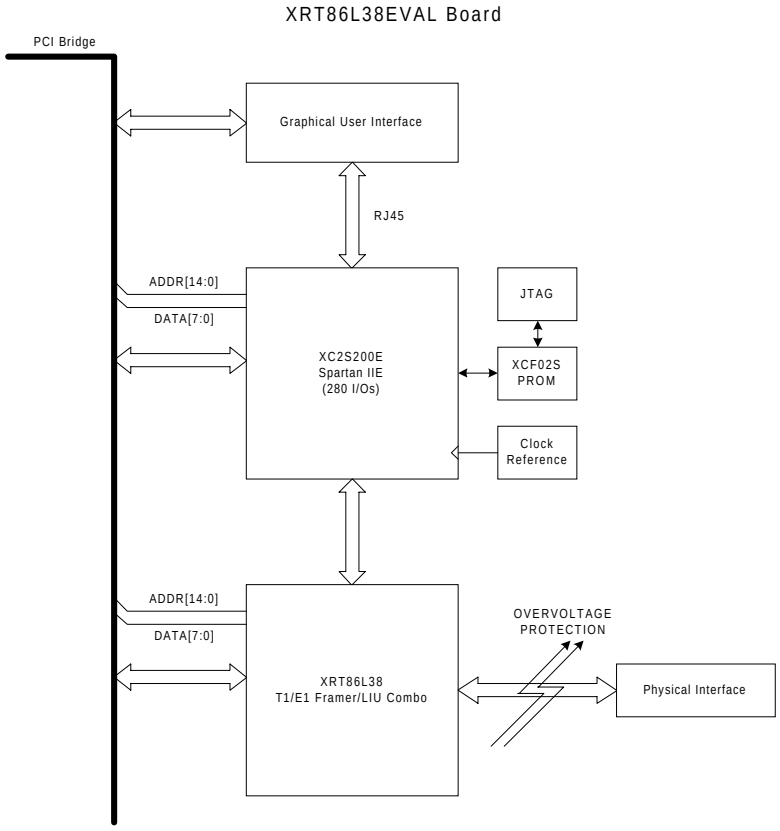


Figure 1 Simplified Block Diagram of the XRT86L38EVAL Application Board

APPLICATION CIRCUITRY

FPGA

The XRT86L38EVAL uses an FPGA designed to control the Framer/LIU and support communication between the PCI bridge and the XRT86L38. The FPGA chosen contains enough I/O pins to support all eight channels with one configuration. By default, the FPGA is configured into an FPGA loopback mode, whereby the output pins from the Framer block are internally looped back to the input pins. This allows standard network equipment connected to the physical interface to monitor data integrity through a complete communication path.

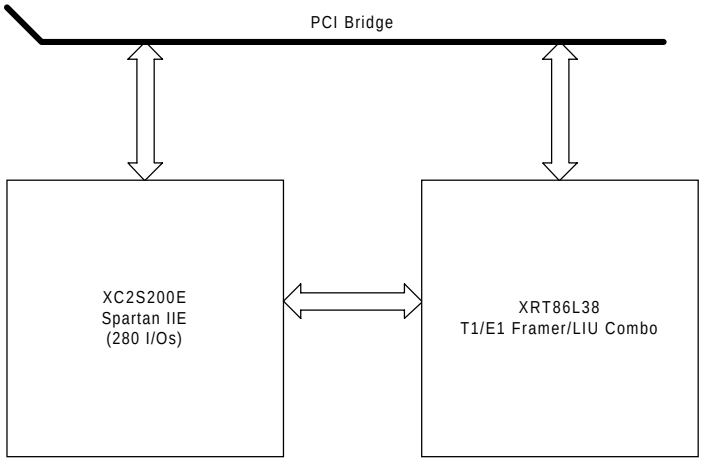


Figure 2 Simplified Block Diagram of the FPGA Interface

Line Interface Module

Internal Impedance

The XRT86L38 has the termination impedance inside the LIU. No termination resistors are necessary for the transmit outputs or the receive inputs. This allows the user to have one bill of materials for all three line impedances. Figure 3 is a simplified block diagram of the interface connection.

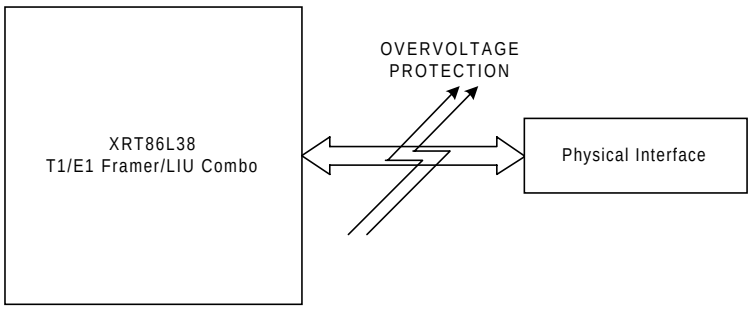
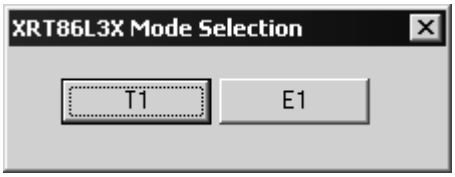


Figure 3 Simplified Block Diagram of the Interface Connection

GRAPHICAL USER INTERFACE (GUI)

INSTALLATION PROCEDURE

The CD ROM contains the necessary files in order to fully evaluate the XRT86L38 evaluation board. By clicking on the "xrt86l3x evaluation vXXX.exe" file, the GUI will automatically install all components. If properly installed,the GUI can be launched from "C:\Program Files\Exar\XRT86L3X Evaluation Software". Once the GUI is launched, the user is given a choice to launch the GUI in either T1 or E1 mode.



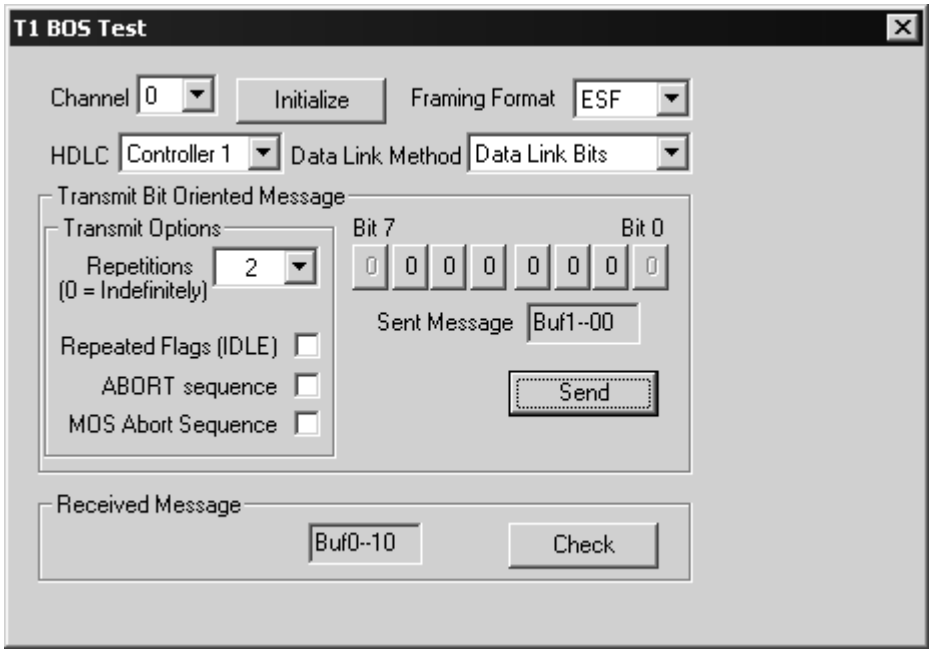
Selecting will load the T1 FPGA or the E1 FPGA, respectively. The user is then presented with this menu.

T1 TEST MENU

The Test menu contains the necessary GUI for testing Bit-Oriented Signaling, Message-Oriented Signaling, Robbed Bit Signaling and Alarm & PMON Monitoring. In order to test these features, it is necessary to place the device in a Framer Local Loopback or an External Loopback by shorting Ttip/Tring to Rtip/Rring through the RJ45 connectors. Also, one should deselect the FPGA loopback in “General Configuration” from the “Configuration” menu.

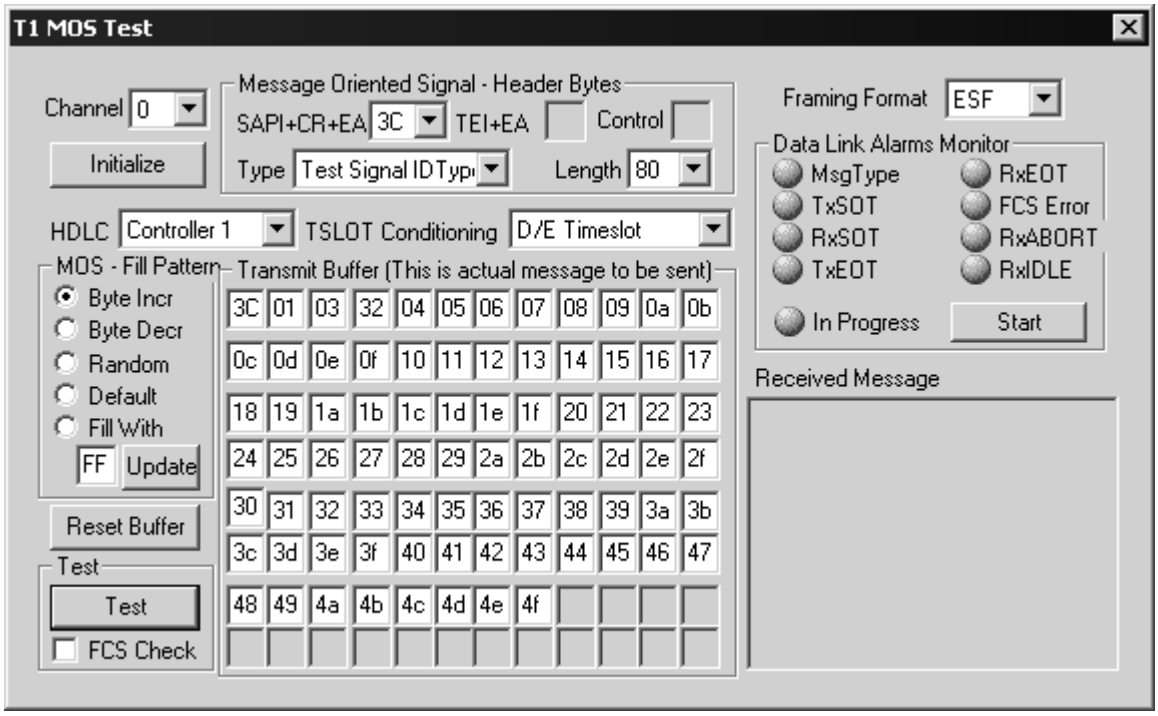
T1 BIT ORIENTED SIGNALING

In order to Test BOS, select the desired channel, select a framing format that supports BOS such as ESF and ensure Controller 1 and Data Link Bits are used. Then click Send.



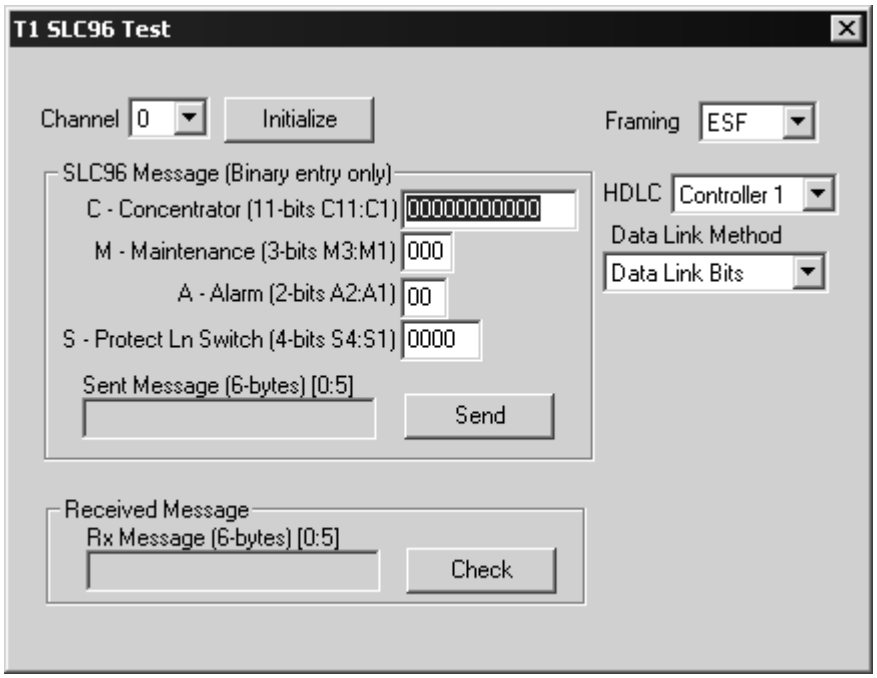
T1 MESSAGE ORIENTED SIGNALING

In order to Test MOS, select a framing format that supports MOS, select a Fill Pattern, select a TSLOT conditioning (note that D/E Timeslot can be used with practically al framing formats) and select a HDLC Controller (Controller 1 must be used when using Data Link Bits). Then click Start which begins the process of checking for received messages. Click Test to send the message.



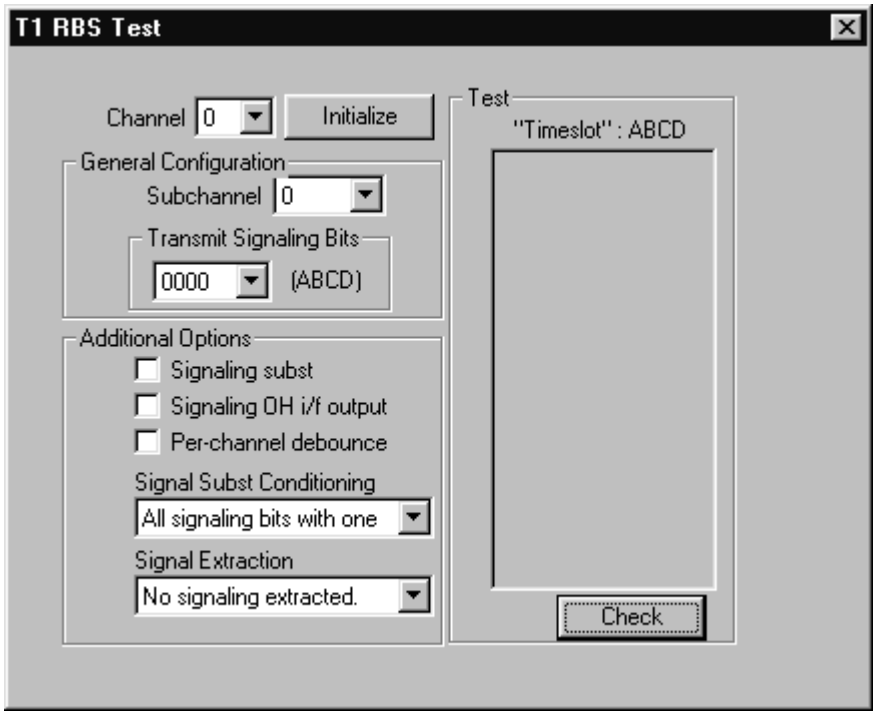
T1 SLC96 Test

In Order SLC96, ensure the framing format is SLC96, modify the SLC96 message to your liking. Other settings can be left at default. Then click Send. Click Check to check for received messages.

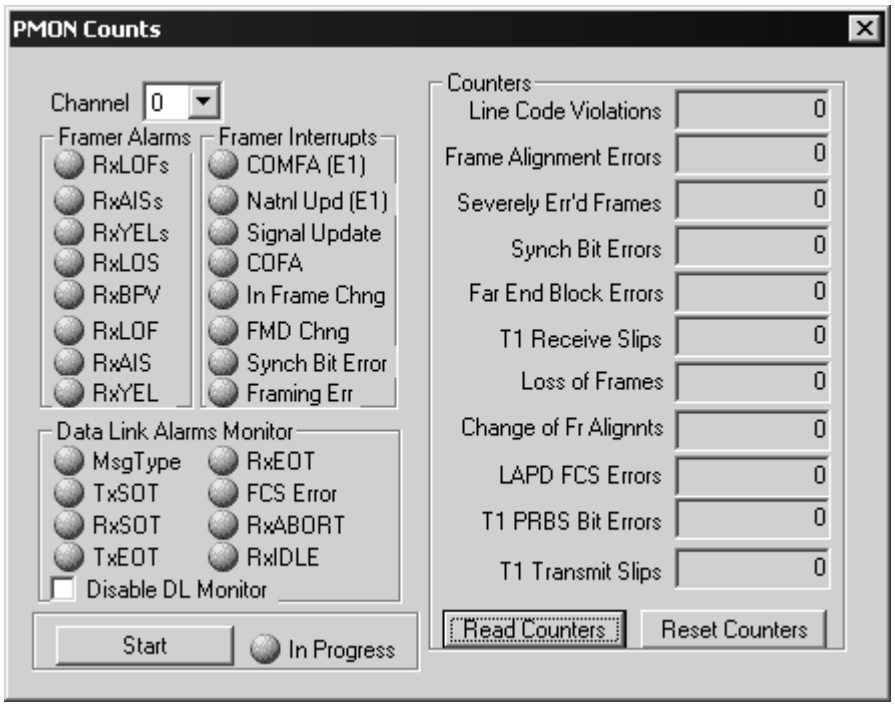


T1 ROBBED BIT SIGNALING MENU

In order to Test RBS, select the desired channel, and then Subchannel (Time Slot) to be configured. Once the desired time slot is selected, the transmit signaling bits can be programmed. This menu is used in conjunction with the "T1 Specific" page from the "General Configuration Menu".

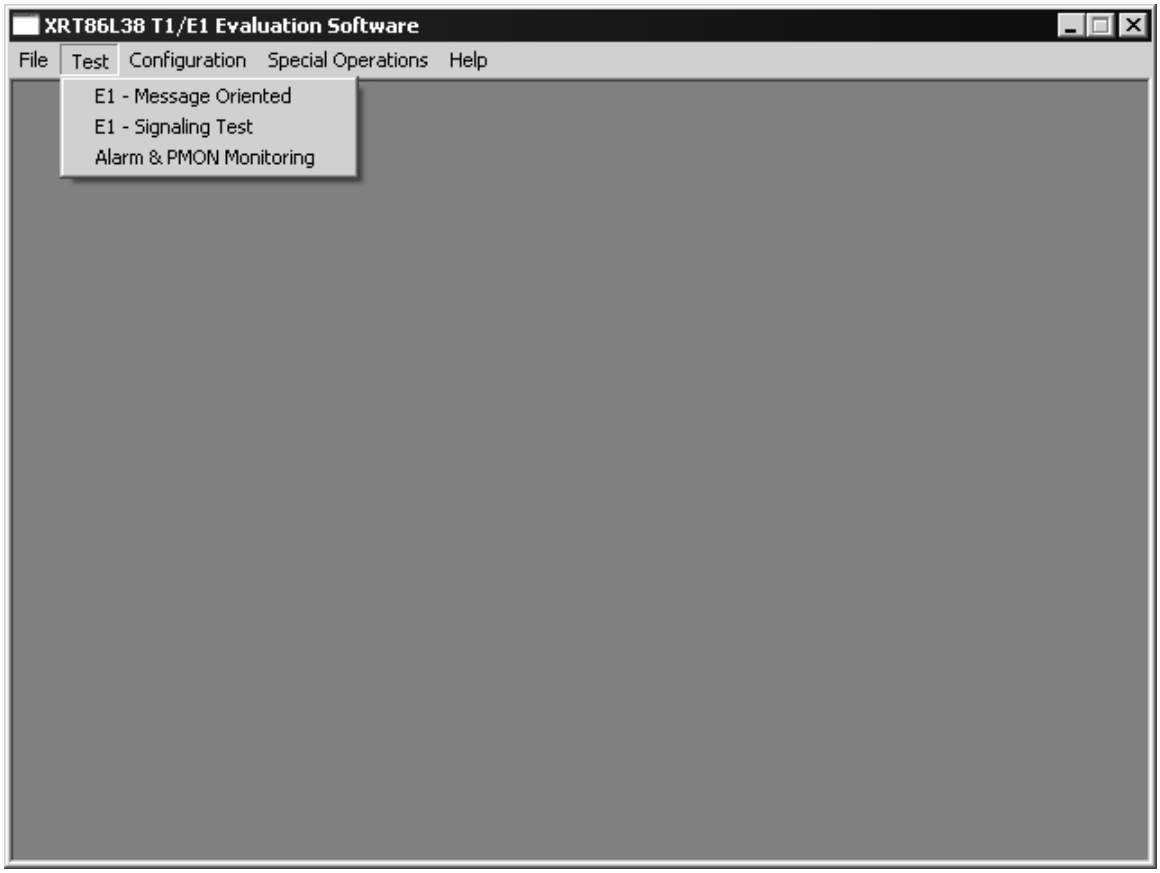


ALARM & PMON MONITORING



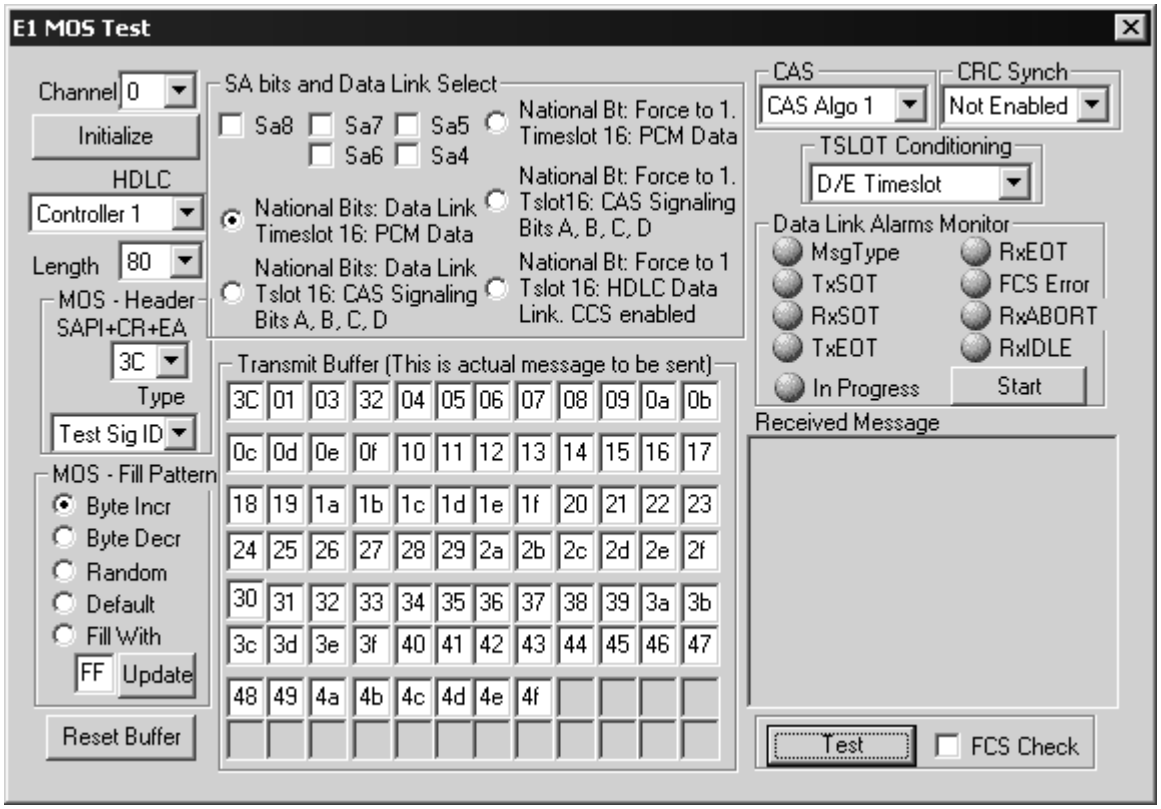
E1 TEST MENU

The Test menu contains the necessary GUI for testing Message-Oriented Signaling, CAS Signaling and Alarm & PMON Monitoring. In order to test these features, it is necessary to place the device in a Framer Local Loopback or an External Loopback by shorting Ttip/Tring to Rtip/Rring through the RJ45 connectors. Also, one should deselect the FPGA loopback in "General Configuration" from the "Configuration" menu.



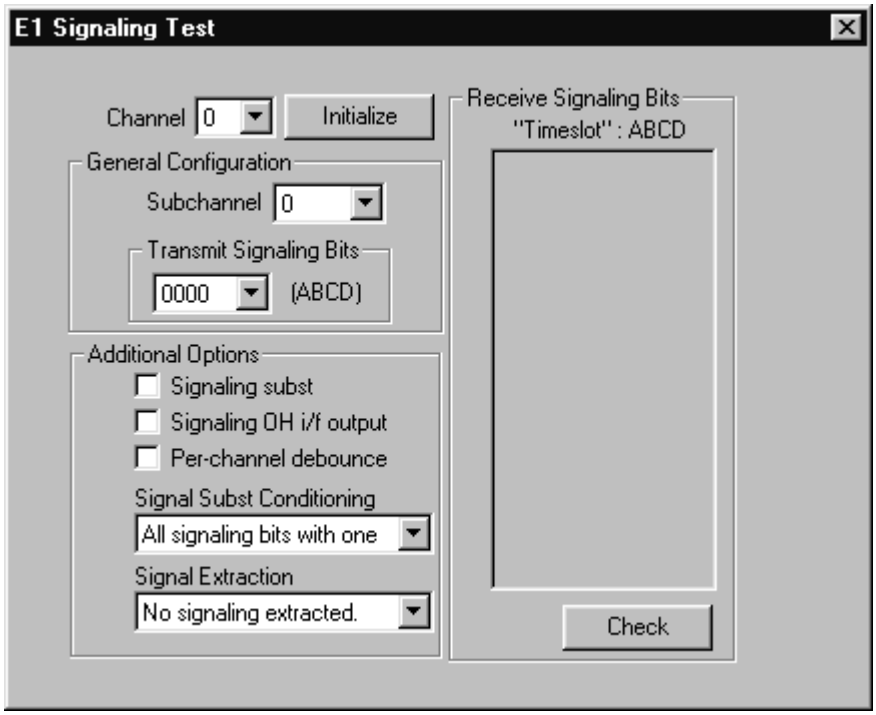
E1 MESSAGE ORIENTED SIGNALING

In order to Test MOS, select a framing format that supports MOS, select a Fill Pattern, select a TSLOT conditioning (note that D/E Timeslot can be used with practically al framing formats) and select a HDLC Controller (Controller 1 must be used when using Data Link Bits). Then click Start which begins the process of checking for received messages. Click Test to send the message.

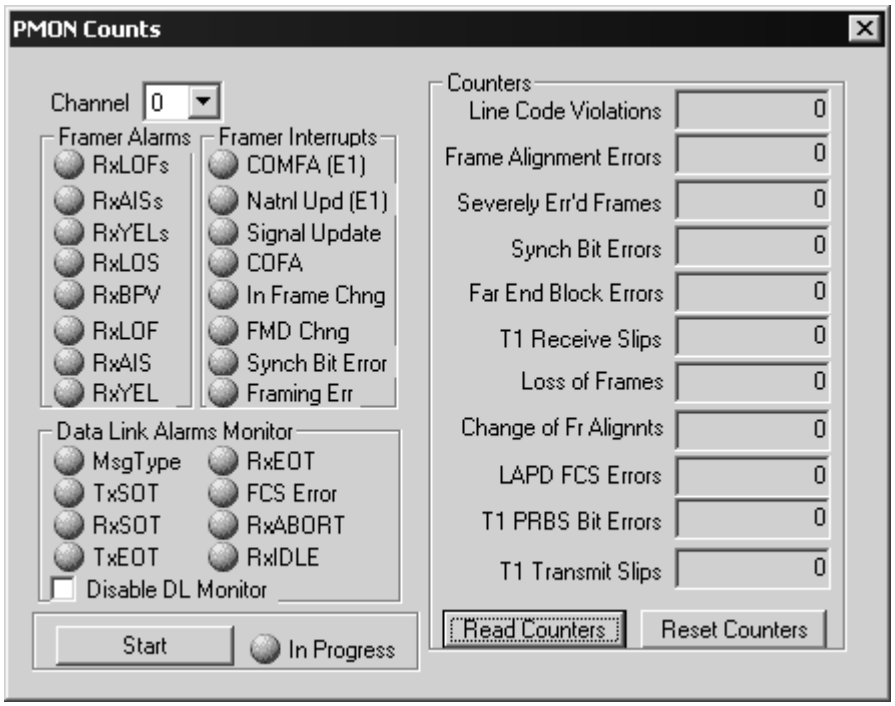


E1 SIGNALING TEST

In order to Test Signaling, select the desired channel, and then Subchannel (Time Slot) to be configured. Once the desired time slot is selected, the transmit signaling bits can be programmed. This menu is used in conjunction with the "E1 Specific" page from the "General Configuration Menu".



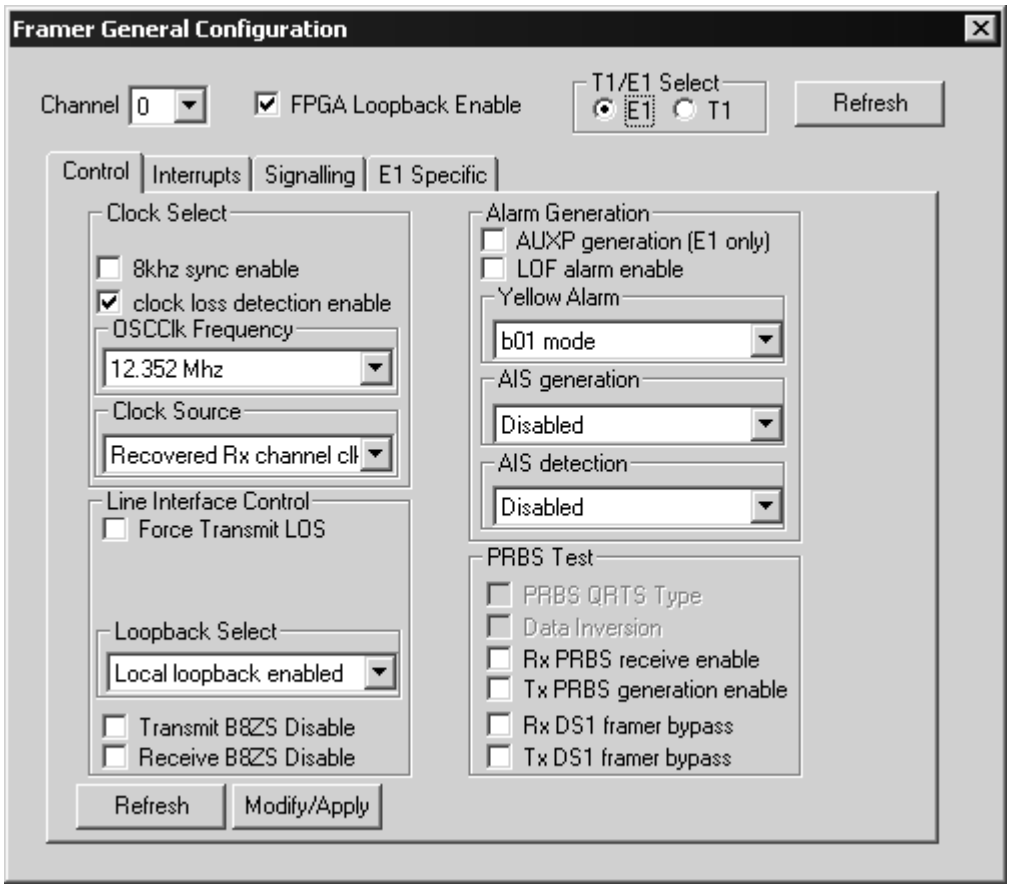
ALARM & PMON MONITORING

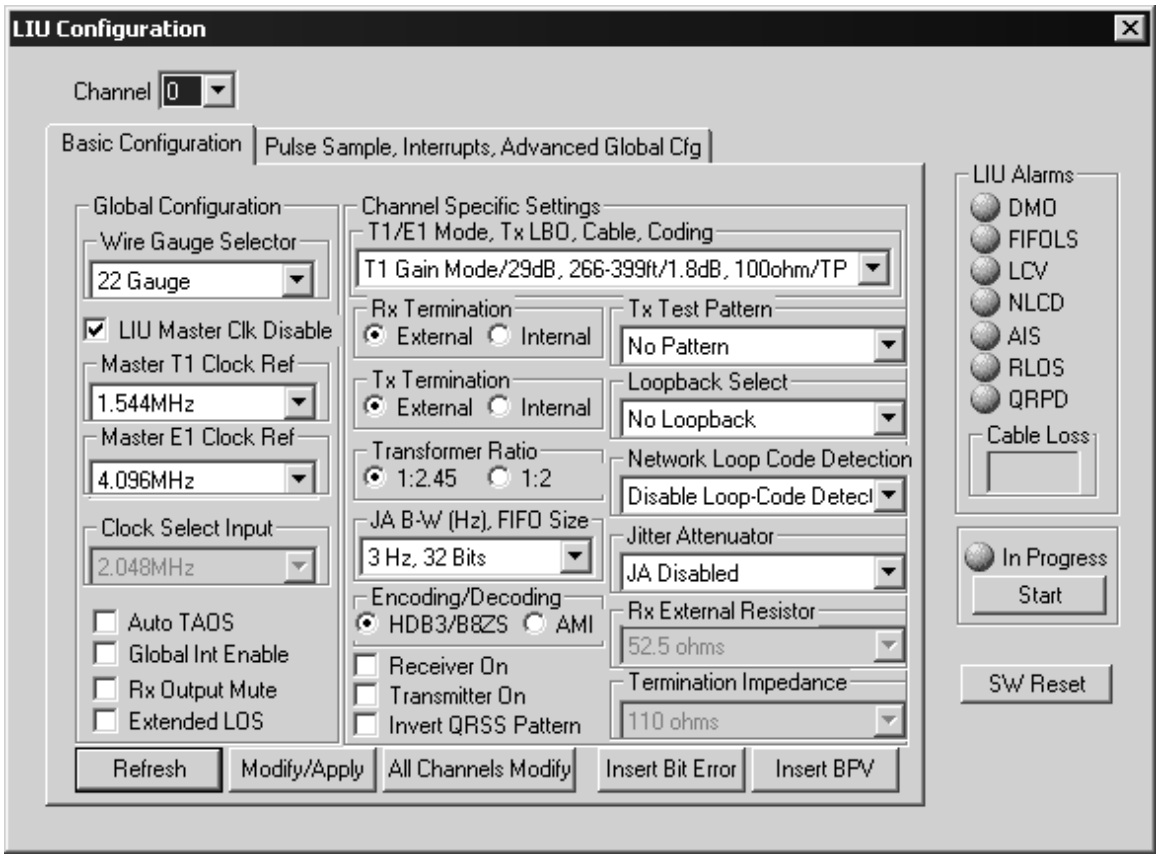


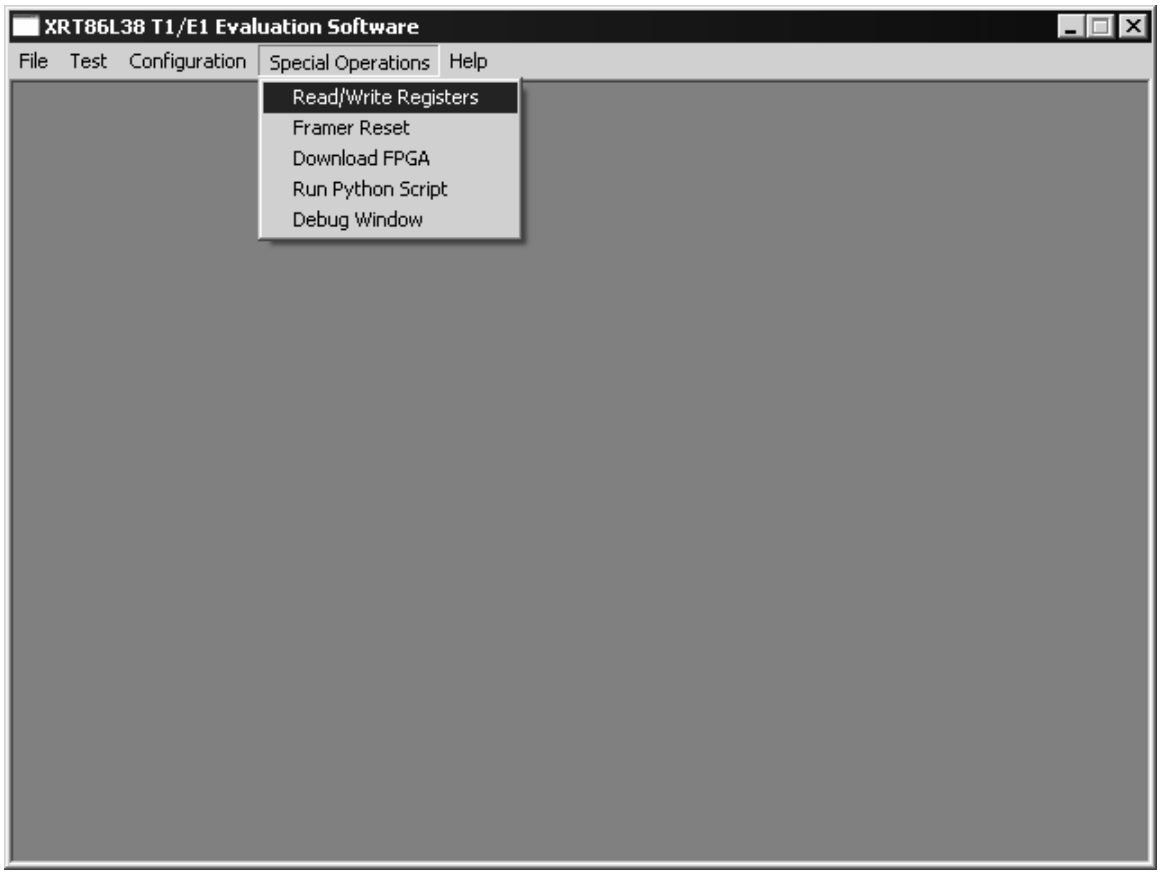
CONFIGURATION MENU

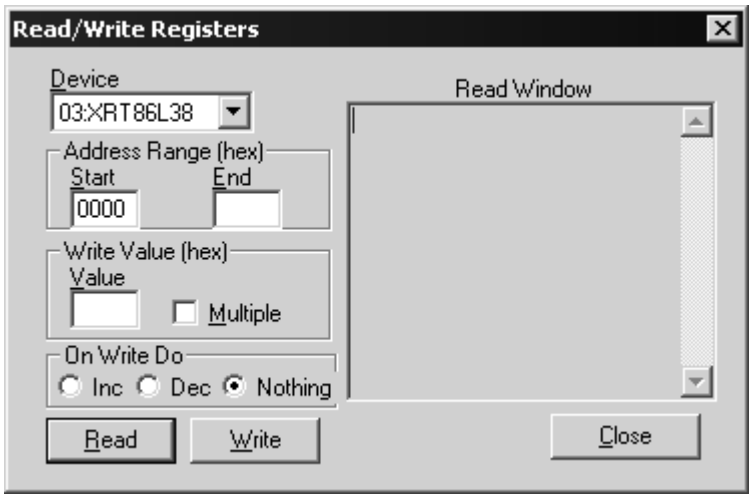
The Configuration menu allows the user to provision the device into common modes for the Framer and LIU sections of the combo chip.


XRT86L38 T1/E1 Evaluation Software
File
Test
Configuration
Special Operations
Help
General Configuration
LIU Configuration


Framer General Configuration
Channel 0
FPGA Loopback Enable
T1/E1 Select
E1
T1
Refresh
Control
Interrupts
Signalling
E1 Specific
Clock Select
8khz sync enable
clock loss detection enable
OSCClk Frequency
12.352 Mhz
Clock Source
Recovered Rx channel clk
Line Interface Control
Force Transmit LOS
Loopback Select
Local loopback enabled
Transmit B8ZS Disable
Receive B8ZS Disable
Alarm Generation
AUXP generation (E1 only)
LOF alarm enable
Yellow Alarm
b01 mode
AIS generation
Disabled
AIS detection
Disabled
PRBS Test
PRBS QRTS Type
Data Inversion
Rx PRBS receive enable
Tx PRBS generation enable
Rx DS1 framer bypass
Tx DS1 framer bypass
Refresh
Modify/Apply


LIU Configuration
Channel 0
Basic Configuration
Pulse Sample, Interrupts, Advanced Global Cfg
Global Configuration
Wire Gauge Selector
22 Gauge
LIU Master Clk Disable
Master T1 Clock Ref
1.544MHz
Master E1 Clock Ref
4.096MHz
Clock Select Input
2.048MHz
Auto TAOS
Global Int Enable
Rx Output Mute
Extended LOS
Channel Specific Settings
T1/E1 Mode, Tx LBO, Cable, Coding
T1 Gain Mode/29dB, 266-399ft/1.8dB, 100ohm/TP
Rx Termination
External
Internal
Tx Termination
External
Internal
Transformer Ratio
1:2.45
1:2
JA B-W (Hz), FIFO Size
3 Hz, 32 Bits
Encoding/Decoding
HDB3/B8ZS
AMI
Receiver On
Transmitter On
Invert QRSS Pattern
Tx Test Pattern
No Pattern
Loopback Select
No Loopback
Network Loop Code Detection
Disable Loop-Code Detecl
Jitter Attenuator
JA Disabled
Rx External Resistor
52.5 ohms
Termination Impedance
110 ohms
Refresh
Modify/Apply
All Channels Modify
Insert Bit Error
Insert BPV
LIU Alarms
DMO
FIFOLS
LCV
NLCD
AIS
RLOS
QRPD
Cable Loss
In Progress
Start
SW Reset


XRT86L38 T1/E1 Evaluation Software
File
Test
Configuration
Special Operations
Help
Read/Write Registers
Framer Reset
Download FPGA
Run Python Script
Debug Window


Read/Write Registers
Device
03:XRT86L38
Address Range (hex)
Start
End
0000
Write Value (hex)
Value
Multiple
On Write Do
Inc
Dec
Nothing
Read
Write
Read Window
Close

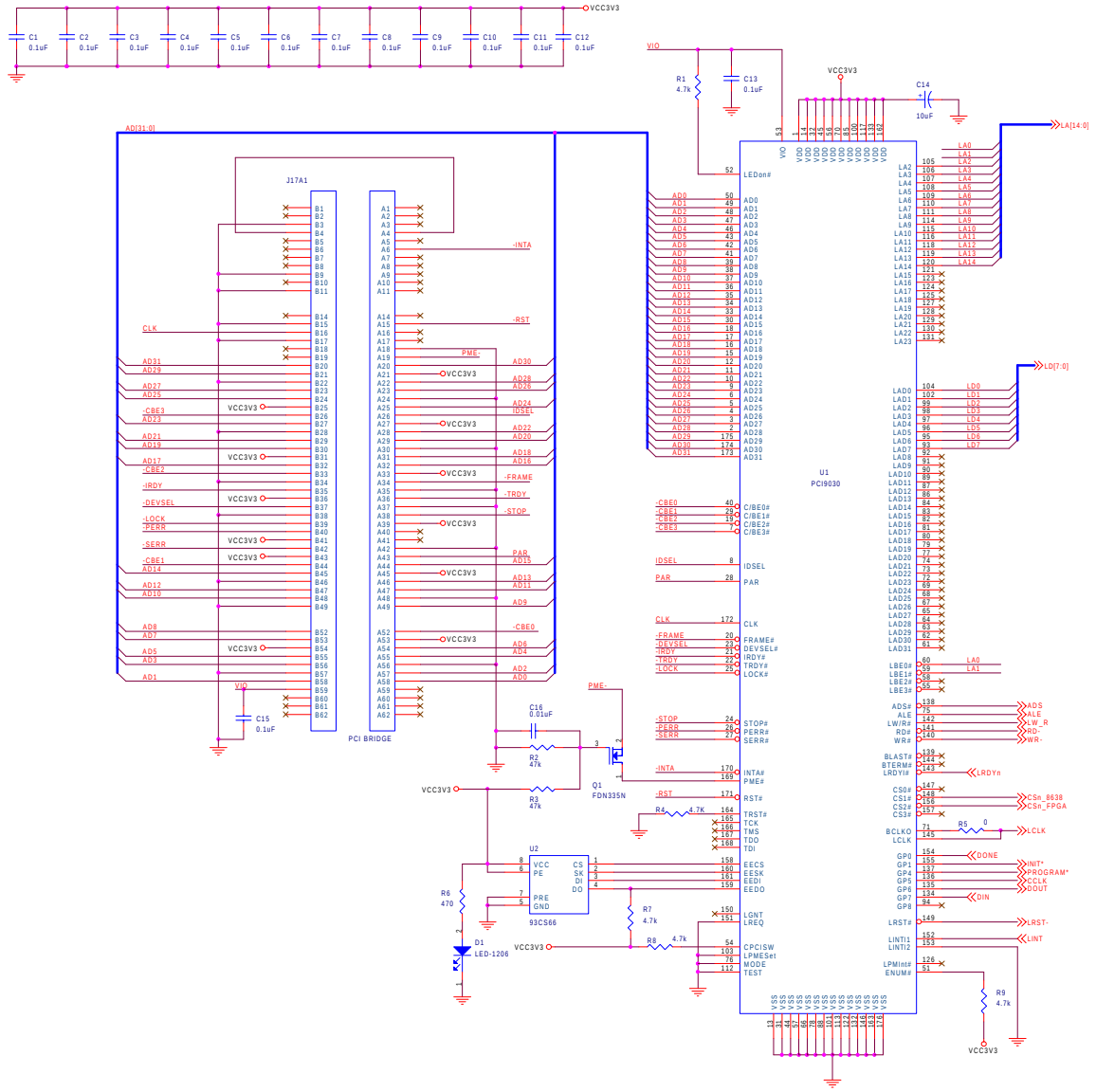


Figure 4 XRT86L38EVAL PCI Bridge (Schematic Page 1)

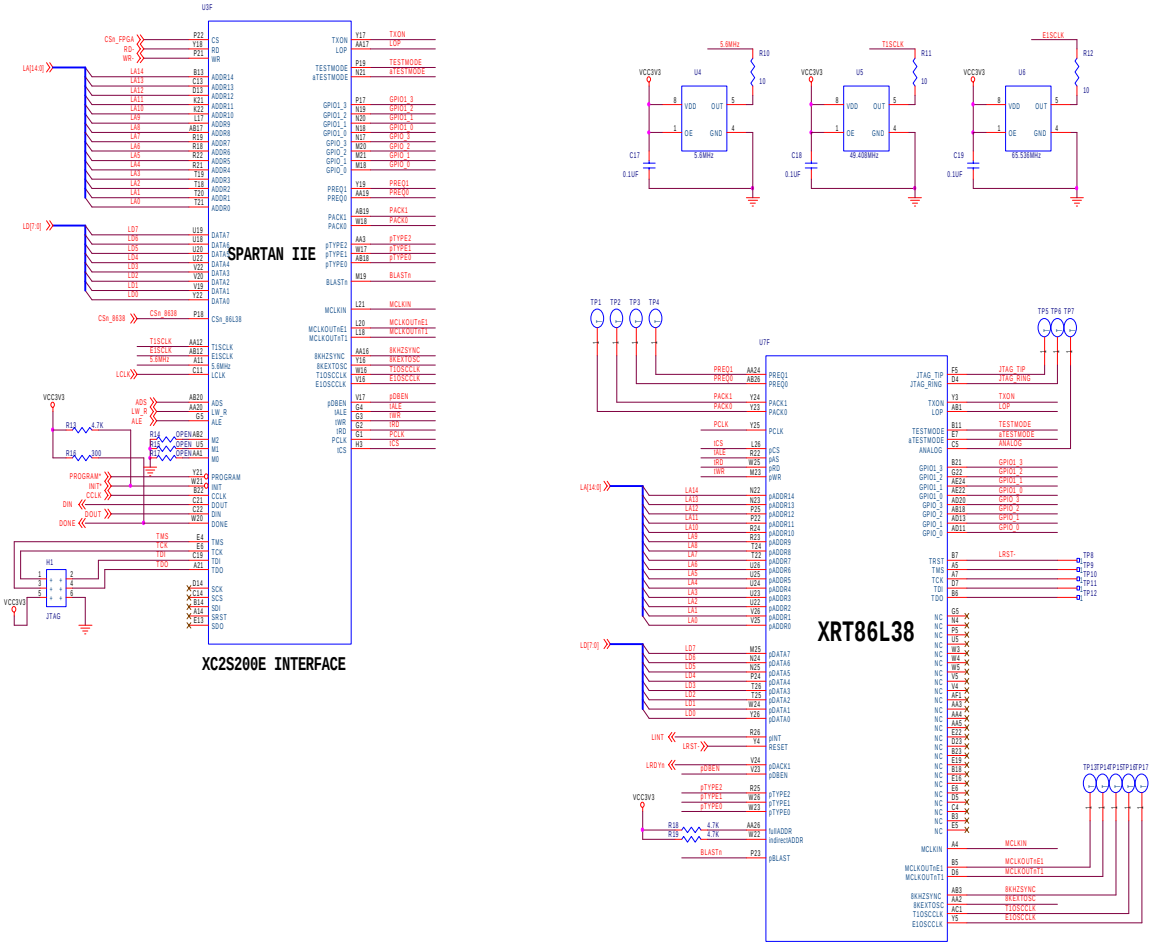


Figure 5 XRT86L38EVAL FPGA Control (Schematic Page 2)

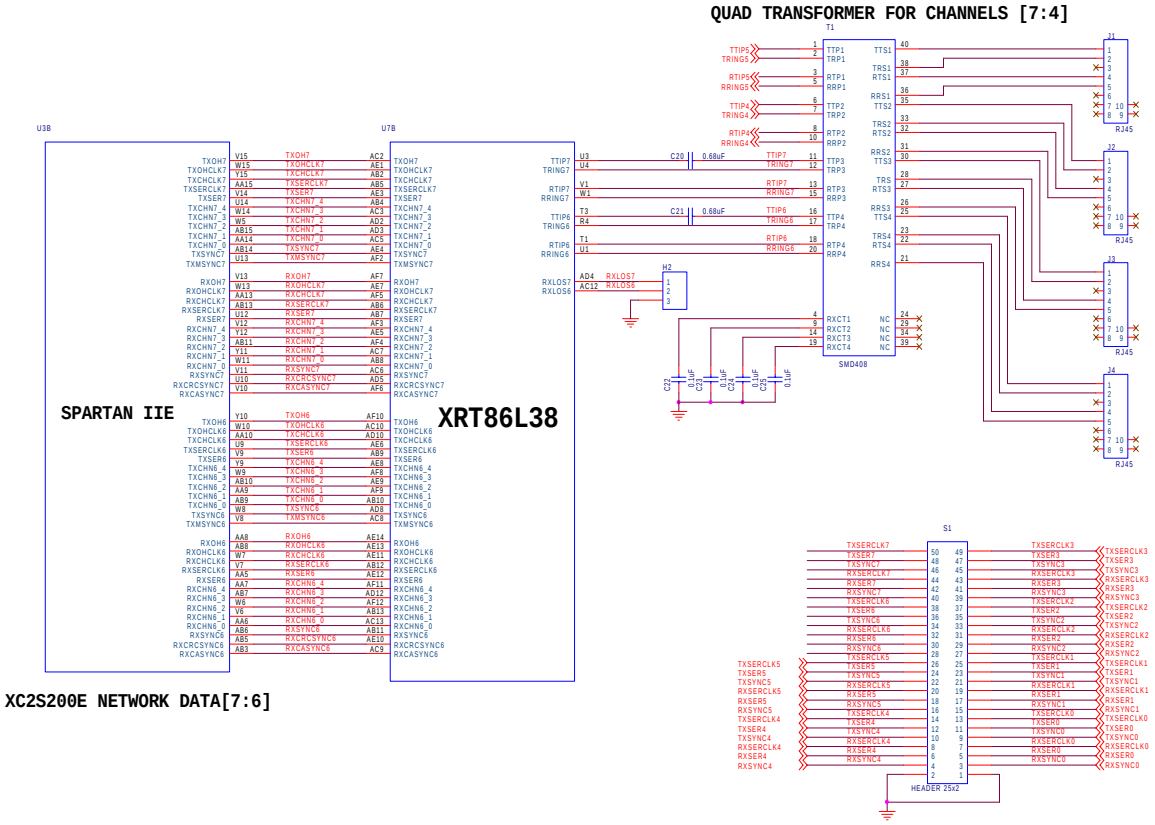
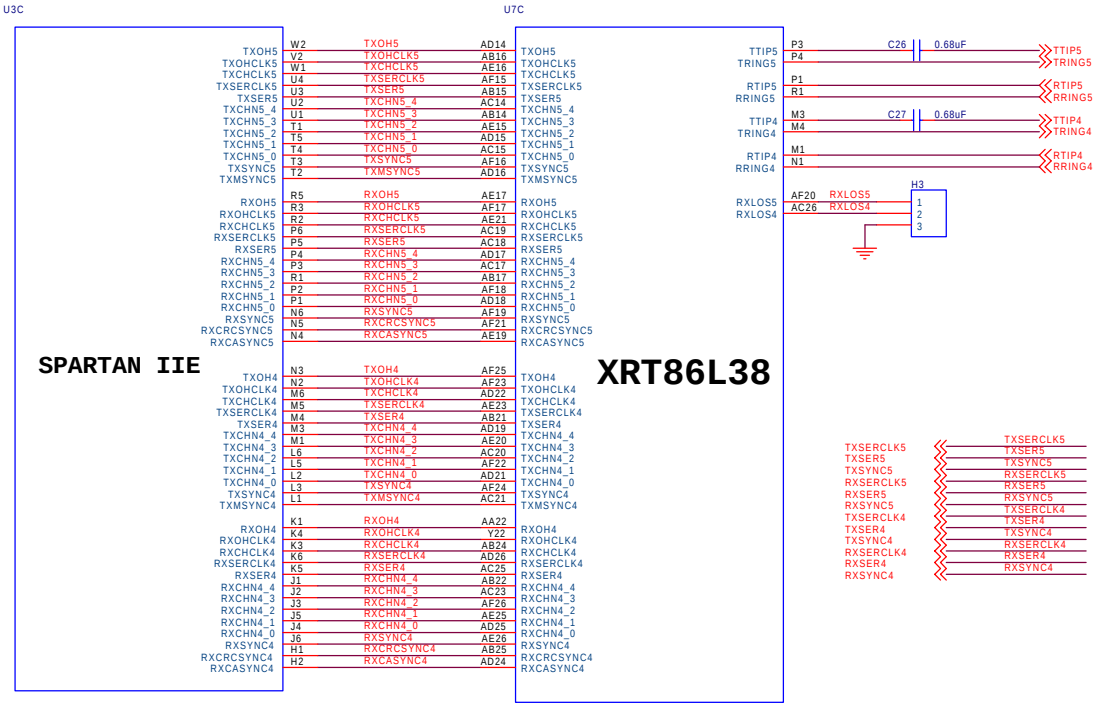


Figure 6 XRT86L38EVAL FPGA Channel Control (Schematic Page 3)



XC2S200E FRAMER BLOCK[5:4]

Figure 7 XRT86L38EVAL FPGA Channel Control (Schematic Page 4)

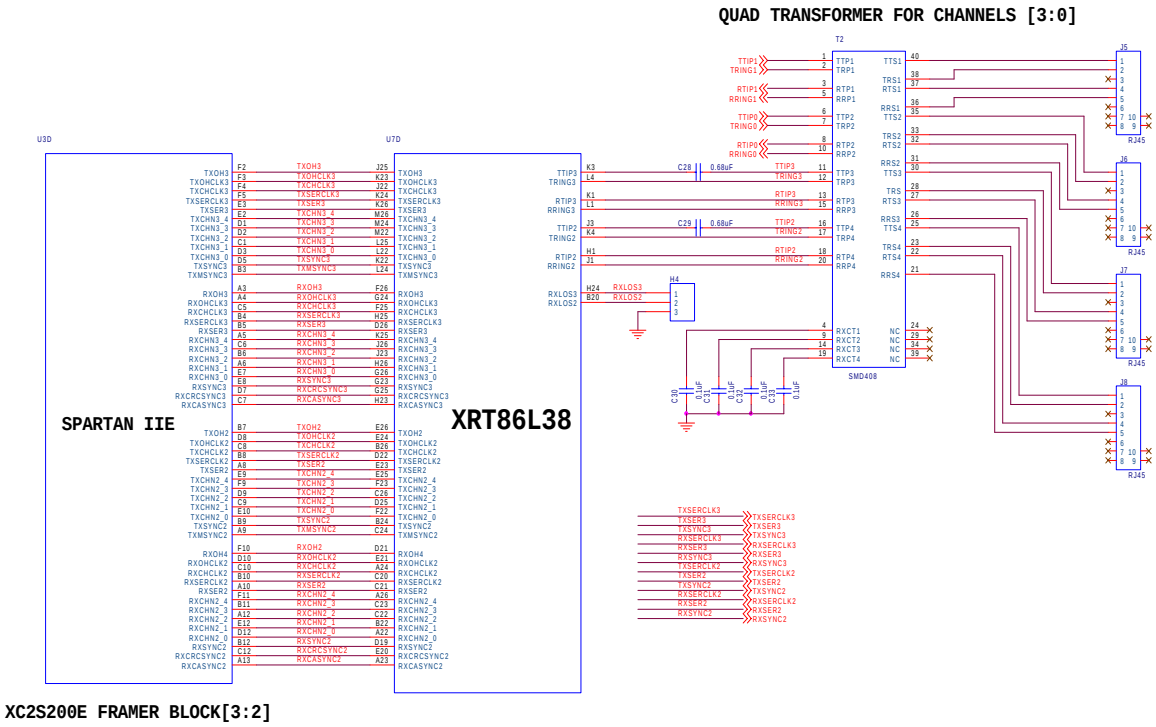


Figure 8 XRT86L38EVAL FPGA Channel Control (Schematic Page 5)

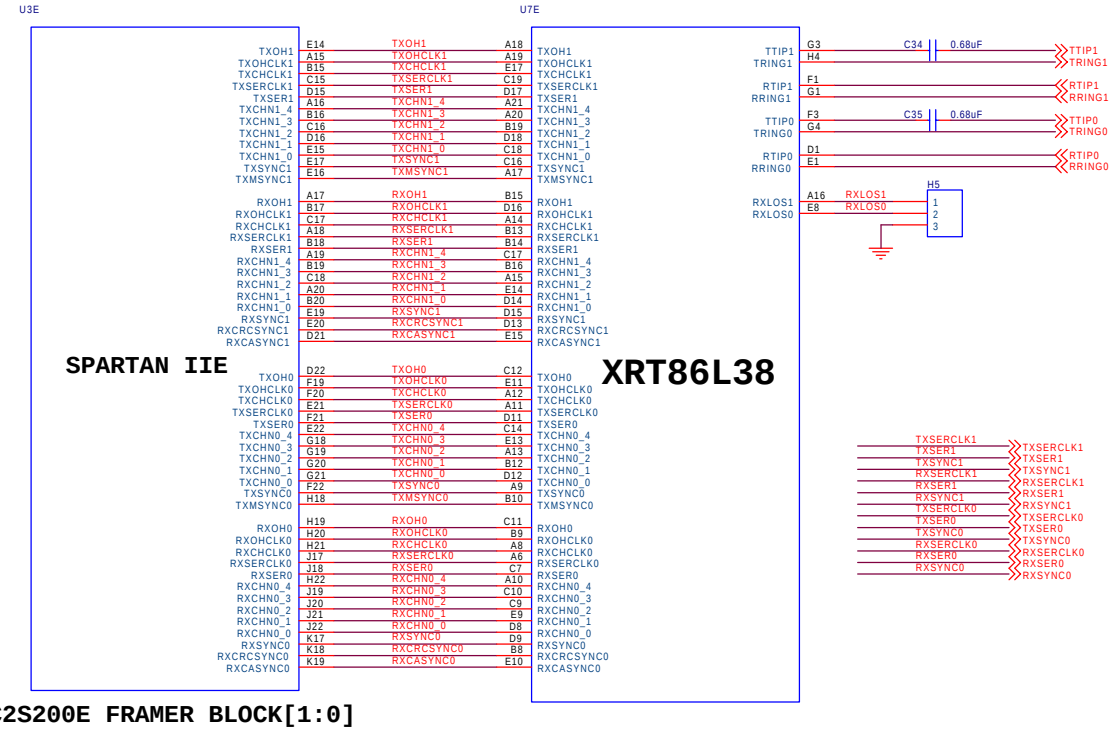


Figure 9 XRT86L38EVAL FPGA Channel Control (Schematic Page 6)

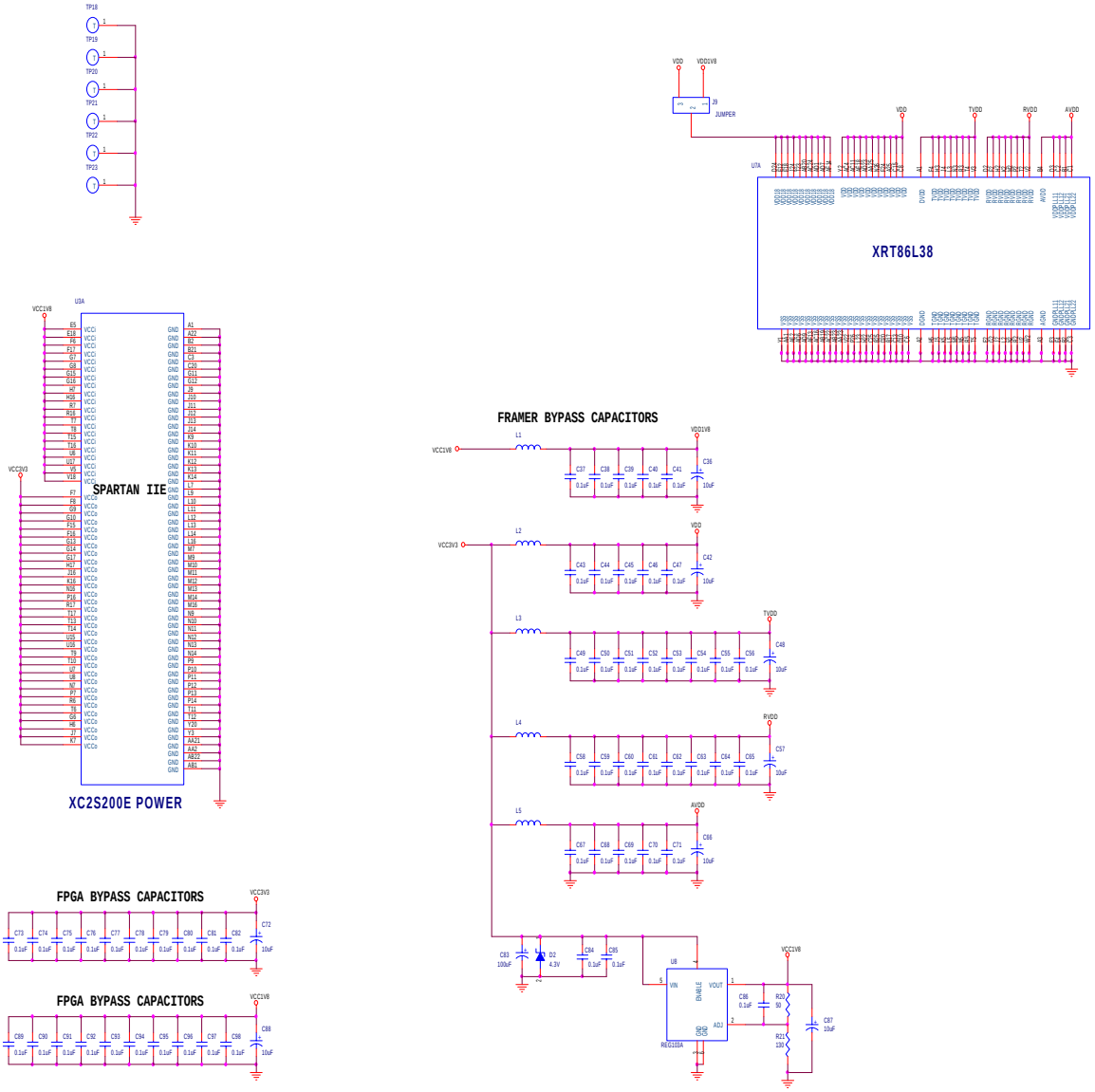


Figure 10 XRT86L38EVAL Power Supply Design (Schematic Page 7)

Layout Recommendations

RTIP/RRING Traces (Long Haul Applications)
The most critical traces are those routed for the receiver inputs in Long Haul applications, where the input may be attenuated up to –42dB of cable loss. The differential pair of each channel should be isolated from other signals on the PCB to prevent unwanted crosstalk or interference. TTIP and TRING transmit an output at full power (0 dB) and should be routed with at least 10 mil spacing away from the receive signals.

Center Tap Capacitor on the Transformer
For best performance, it is recommended that the center tap of the receive transformer be bypassed to ground with a 0.1uF capacitor if a center tap is available. The capacitor will help filter out noise that otherwise could be AC coupled from the line interface through the transformer.

TVDD
Transmit Analog Power Supply (3.3V ±5%)

TVDD can be shared with DVDD. However, it is recommended that TVDD be isolated from the analog power supply RVDD. For best results, use an internal power plane with copper pour separation. If an internal power plane is not available, a ferrite bead can be used. Each power supply pin should be bypassed to ground through an external 0.1μF capacitor.

RVDD
Receive Analog Power Supply (3.3V ±5%)

For long haul applications, RVDD should not be shared with other power supplies. It is recommended that RVDD be isolated from the digital power supply DVDD and the analog power supply TVDD. For best results, use an internal power plane with copper pour separation. If an internal power plane is not available, a ferrite bead can be used. Each power supply pin should be bypassed to ground through an external 0.1μF capacitor.

> *Note: In long haul applications where the receive inputs can be severely attenuated, it is critical to have a clean power supply design and clean PCB layout with respect to RVDD. It is highly recommended that RVDD be isolated from DVDD and TVDD.*

DVDD
Digital Power Supply (3.3V ±5%)

DVDD should be isolated from the analog power supplies. For best results, use an internal power plane with copper pour separation. If an internal power plane is not available, a ferrite bead can be used. Every two DVDD power supply pins should be bypassed to ground through at least one 0.1μF capacitor.

AVDD
Analog Power Supply (3.3V ±5%)

AVDD should be isolated from the digital power supplies. For best results, use an internal power plane with copper pour separation. If an internal power plane is not available, a ferrite bead can be used. Each power supply pin should be bypassed to ground through at least one 0.1μF capacitor.

GND
It's recommended that all ground pins of this device be tied together at one common ground point.